AMD Family 11h Processor Power and Thermal Data Sheet for Notebooks

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Revision History

Date	Revision	Description
September 2008	3.00	Initial public release

1 Overview

This document contains processor thermal specifications and power specifications. The specifications in this document supersede those found in the power roadmaps. For all other electrical specifications, refer to the appropriate product data sheet and the *AMD Family 11h Processor Electrical Data Sheet*, order# 40683.

1.1 Organization

This document is organized into the following sections:

- Document overview (Section 1)
- One section for each brand represented in the mobile segment containing the following subsections:
  - Ordering Part Number (OPN) description (content overview in Section 1.1.1)
  - Thermal and power specification tables (content overview in Section 1.1.3 on page 9)
- Power supply specifications (content overview in Section 1.1.4 on page 9)
- **MTOPS** section in Table 32 on page 43
- **APP** section in Table 33 on page 44

1.1.1 Ordering Part Number Description Section Overview

The Ordering Part Number (OPN) description section contains a depiction and description of a valid OPN for the brand contained in that chapter. Each character or group of characters within an OPN has a specific meaning (for example, model number, socket compatibility). The meaning of each OPN character is detailed in the OPN description section. Each OPN identifies a processor with a unique thermal and power specification table entry.

The OPN description section also contains a full description of the Subsection Ordering Part Number (SOPN) abstraction characters for the brand contained in that chapter. SOPNs are used to group and organize OPNs into subsections for the thermal and power tables and power supply specifications. A definition of SOPNs is contained in Section 1.3 on page 9.

1.1.2 Thermal and Power Table Guide Overview

The thermal and power table guide section contains a table mapping SOPNs and the properties associated with their defined characters to the proper thermal and power table subsections and page numbers. This table is designed to be used as a quick reference for finding the appropriate subsection for the thermal and power tables corresponding to an SOPN.

1.1.3 Thermal and Power Table Section Overview

The thermal and power specification tables contain the thermal and power requirements for each OPN. This includes the information necessary for thermal management (for example, heat sink requirements, ambient temperature assumptions) and power delivery (for example, voltage and current, and power dissipation for each P-state).

The thermal and power specification tables are organized into subsections that correspond to Subsection Ordering Part Numbers (SOPNs). SOPNs for the thermal and power tables have the brand, power limit, and part definition characters defined in the form **AB**mmmmrrpnc **GH**. Each chapter provides a guide table that maps the SOPNs in the thermal and power tables within that chapter to the appropriate subsection number and page number. Within each subsection the OPNs are sorted by model number, socket compatibility, voltage, temperature, and cache size, respectively.

1.1.4 Power Supply Specification Chapter Overview

The power supply specification chapter contains the operating conditions and requirements for all voltage planes required by the processor.

1.2 Conventions

Following are conventions used with numbers.

- Binary numbers. A “b” appended to the end of a number indicates that it is a binary number, for example: 0110b.
- Decimal numbers. Unless specified otherwise, all numbers are decimal.
- Hexadecimal numbers. An “h” appended to the end of a number indicates that it is a hexadecimal number, for example: 45F8h.
- Underscores in numbers. Underscores are used to break up numbers to make them more readable, for example: 0110_1100b. They do not imply any operation.

1.3 Definitions

Following are some key definitions.

- **CPU COF**. CPU Current Operating Frequency.
- **NB COF**. Northbridge (NB) Current Operating Frequency.
- **OPN**. Ordering Part Number. An OPN uniquely identifies a processor and its associated specifications in the thermal and power tables and power supply specifications section.
- **P-state**. Processor Performance State. P-states are valid combinations of CPU voltage, CPU COF, Northbridge voltage, and NB COF.

- **SOPN**. Subsection Ordering Part Number. An SOPN is an OPN with a subset of defined characters. All defined characters in an SOPN are bolded and capitalized. All abstracted characters in an SOPN are in non-bolded lowercase. Information for any OPN that matches all of the defined characters in an SOPN is contained in that subsection. For example, OPN AB1234CDE5FGH appears under the subsection for SOPN **AB**mmmmrrpnc**GH**. The abstracted (lower-case) character definitions for SOPNs are contained in the OPN description section of each chapter.
- **State**. Indicates the ACPI defined sleep state, power state, and performance state for the related specifications. An ‘x’ indicates the related specifications are independent of the associated ACPI state. For example, S0.C0.P0 indicates Sleep state 0, Power state 0, and Performance state 0. S3.Cx.Px indicates Sleep state 3 entered from any power and performance state combination.
- **TDC**. Thermal Design Current. The thermal design current is the sustained current limit as measured under the same conditions as TDP.
- **TDP**. Thermal Design Power. The thermal design power is the maximum power a processor can draw for a thermally significant period while running commercially useful software. The constraining conditions for TDP are specified in the notes in the thermal and power tables.
- **Triple-plane.** Platforms in which the VDD0 (core 0), VDD1 (core 1) and VDDNB (Northbridge) planes are isolated on the platform and controlled as separate voltages through the SVI interface.
- **VID_VDD**. The VID_VDD voltage is the VID-requested VDD supply level. Refer to the *BIOS and Kernel Developer’s Guide (BKDG) for AMD Family 11h Processors*, order# 41256, for VID-to-voltage translation specifications.

2 AMD Turion™ X2 Ultra Dual-Core Mobile Processor

The following sections contain the OPN description and thermal and power specifications for the AMD Turion™ X2 Ultra dual-core mobile processor. Each column in the thermal and power tables represents a specific Ordering Part Number (OPN). Section 2.1 provides an example of the OPN structure for this processor family.

2.1 AMD Turion™ X2 Ultra Dual-Core Mobile Processor Ordering Part Number Description

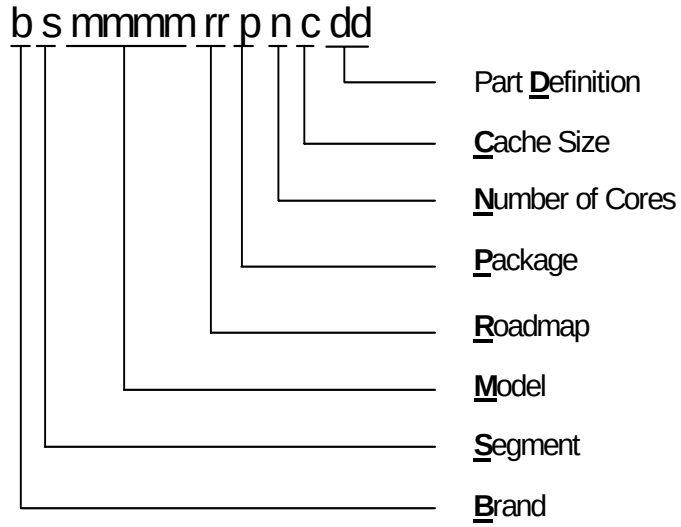

Figure 1. AMD Turion™ X2 Ultra Dual-Core Mobile Processor Ordering Part Number Diagram

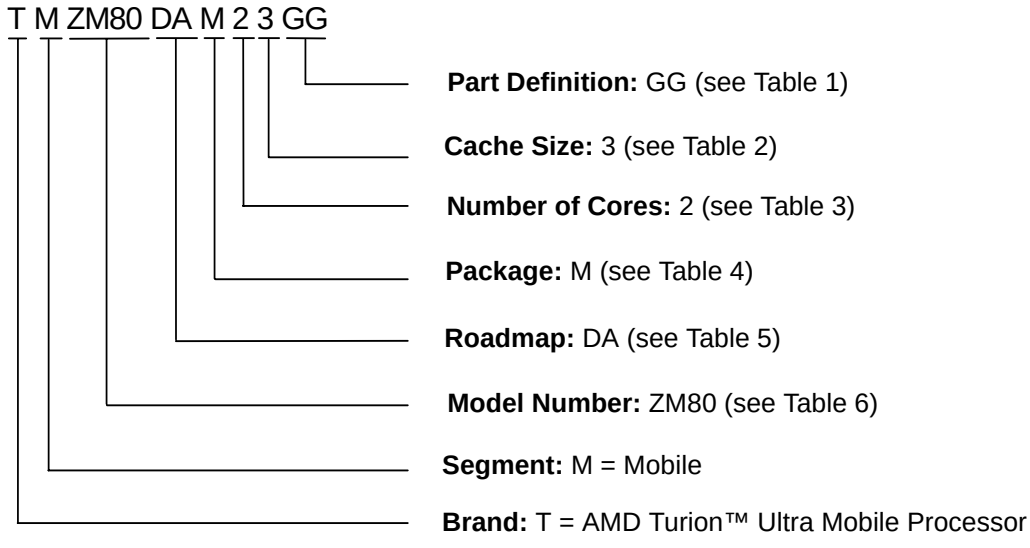

Figure 2. AMD Turion™ X2 Ultra Dual-Core Mobile Processor Ordering Part Number Example

Table 1. AMD Turion™ X2 Ultra Dual-Core Mobile Processor Part Definition Options

Part Definition	Revision	CPUID 8000_0001h EAX [31:0] (CPUID)
GG	Rev B1	00200F31h

Table 2. AMD Turion™ X2 Ultra Dual-Core Mobile Processor L2 Cache Size Options

OPN Character	L2 Cache Size
3	1024 KB

Table 3. AMD Turion™ X2 Ultra Dual-Core Mobile Processor Number of Cores

OPN Character	Number of Cores
2	2

Table 4. AMD Turion™ X2 Ultra Dual-Core Mobile Processor Package Options

OPN Character	Package
M	S1g2

Table 5. AMD Turion™ X2 Ultra Dual-Core Mobile Processor Roadmap Options

OPN Character	Power, Segment	Number of Cores	Socket Infrastructure
DA	35 W, Notebook	2	S1g2

Table 6. AMD Turion™ X2 Ultra Dual-Core Mobile Processor Model Number Options

Frequency	L2 Cache Size	Model Number
2100 MHz	1024 KB	ZM80
2200 MHz	1024 KB	ZM82
2300 MHz	1024 KB	ZM84
2400 MHz	1024 KB	ZM86

2.2 AMD Turion™ X2 Ultra Dual-Core Mobile Processor Thermal and Power Table Guide

The thermal and power table guide shown in Table 7 maps SOPNs and the properties associated with their defined characters to the proper thermal and power table subsections and page numbers. This table is designed to be used as a quick reference for finding the appropriate subsection for the thermal and power tables corresponding to an SOPN.

Table 7. AMD Turion™ X2 Ultra Dual-Core Mobile Processor Thermal and Power Table Guide

SOPN	Power	Revision	Thermal/Power Tables
TM mmmm **DA** pnc **GG**	35 W	Rev B1	Section 2.3.1 on page 15

2.3 AMD Turion™ X2 Ultra Dual-Core Mobile Processor Thermal and Power Specifications

Refer to the *AMD Family 11h Processor Electrical Data Sheet*, order# 40683, for electrical specifications for the processor. Refer to the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors*, order# 41256, for power management BIOS requirements.

Section 2.1 on page 11 provides an example of the OPN structure for processors documented in this chapter and Table 7 on page 13 provides a guide to OPN organization in the following subsections. Refer to Section 1.2 on page 9 and Section 1.3 on page 9 for numbering conventions and terminology definitions used in these tables.

2.3.1 TM mmmm DA pnc GG (35 W Mobile, S1g2) Thermal and Power Specifications

State	Specification[7]	Notes	TMZM80DAM23GG	TMZM82DAM23GG
S0.C0.Px	Tdie Max	13	100 °C	100 °C
	Tambient		0 °C to 35 °C	0 °C to 35 °C
	TRise		10 °C	10 °C
	Thermal Resistance (die-amb)		1.72 °C/W	1.57 °C/W
	Startup P-state		S0.C0.P2	S0.C0.P2
	HTC P-state Limit	5	S0.C0.HTC	S0.C0.HTC
	IDDNB Max		1.61 A	1.61 A
	VID_VDDNB		0.900 V	0.900 V
S0.C0.P0	CPU COF	1	2100 MHz	2200 MHz
	TDP	3,6	32.0 W	35.0 W
	VID_VDD Min	2	1.075 V	1.100 V
	VID_VDD Max	2	1.125 V	1.125 V
	TDC	6	25.6 A	27.8 A
S0.C0.P1	CPU COF	1	1050 MHz	1100 MHz
	TDP	3,6	15.3 W	16.0 W
	VID_VDD Min	2	0.950 V	0.950 V
	VID_VDD Max	2	0.950 V	0.950 V
	TDC	6	11.4 A	12.2 A
S0.C0.P2	CPU COF	1	525 MHz	550 MHz
	TDP	3,6	9.2 W	9.2 W
	VID_VDD Min	2	0.800 V	0.800 V
	VID_VDD Max	2	0.800 V	0.800 V
	TDC	6	5.9 A	5.9 A
S0.C0.HTC	CPU COF	1	800 MHz	850 MHz
	TDP	3,6	22.6 W	24.3 W
	VID_VDD Min	2	1.200 V	1.200 V
	VID_VDD Max	2	1.200 V	1.200 V
	TDC	6	15.1 A	16.5 A
	C1 Halt	9		
	IDD Max		1.19 A	1.19 A
	I/O Power	4,10	3.0 W	3.0 W
	C1E/S1 @ Min P-state	11		
	IDD Max		0.84 A	0.84 A
	I/O Power	4,10	300 mW	300 mW
	C1E/S1 Altvid	14		
	IDD Max		0.69 A	0.69 A
	IDDNB Max		0.14 A	0.14 A
	I/O Power	4,10	300 mW	300 mW
	S3	12		
	I/O Power	8	150 mW	150 mW

The notes for this table are on page 17.

State	Specification[7]	Notes	TMZM84DAM23GG	TMZM86DAM23GG
S0.C0.Px	Tdie Max	13	100 °C	100 °C
	Tambient		0 °C to 35 °C	0 °C to 35 °C
	TRise		10 °C	10 °C
	Thermal Resistance (die-amb)		1.57 °C/W	1.57 °C/W
	Startup P-state		S0.C0.P2	S0.C0.P2
	HTC P-state Limit	5	S0.C0.HTC	S0.C0.HTC
	IDDNB Max		1.61 A	1.61 A
	VID_VDDNB		0.900 V	0.900 V
S0.C0.P0	CPU COF	1	2300 MHz	2400 MHz
	TDP	3,6	35.0 W	35.0 W
	VID_VDD Min	2	1.100 V	1.100 V
	VID_VDD Max	2	1.125 V	1.125 V
	TDC	6	27.8 A	27.8 A
S0.C0.P1	CPU COF	1	1150 MHz	1200 MHz
	TDP	3,6	16.4 W	16.4 W
	VID_VDD Min	2	0.950 V	0.950 V
	VID_VDD Max	2	0.950 V	0.950 V
	TDC	6	12.6 A	12.6 A
S0.C0.P2	CPU COF	1	575 MHz	600 MHz
	TDP	3,6	9.2 W	9.2 W
	VID_VDD Min	2	0.800 V	0.800 V
	VID_VDD Max	2	0.800 V	0.800 V
	TDC	6	5.9 A	5.9 A
S0.C0.HTC	CPU COF	1	850 MHz	900 MHz
	TDP	3,6	24.7 W	24.7 W
	VID_VDD Min	2	1.200 V	1.200 V
	VID_VDD Max	2	1.200 V	1.200 V
	TDC	6	16.9 A	16.9 A
	C1 Halt	9		
	IDD Max		1.19 A	1.19 A
	I/O Power	4,10	3.0 W	3.0 W
	C1E/S1 @ Min P-state	11		
	IDD Max		0.84 A	0.84 A
	I/O Power	4,10	300 mW	300 mW
	C1E/S1 Altvid	14		
	IDD Max		0.69 A	0.69 A
	IDDNB Max		0.14 A	0.14 A
	I/O Power	4,10	300 mW	300 mW
	S3	12		
	I/O Power	8	150 mW	150 mW

The notes for this table are on page 17.

AMD Turion™ X2 Ultra Dual-Core Mobile Processor Thermal and Power Specification Table Notes:

1. *Frequency reported to the OS is rounded to the nearest 100-MHz boundary.*
2. *Variable voltage—any valid voltage between VDD min and VDD max is allowed.*
3. *The processor thermal solution should be designed to accommodate thermal design power (TDP) at Tdie,max. TDP is measured under the conditions of all cores operating at CPU COF, Tdie Max, and VDD at the voltage requested by the processor. TDP includes all power dissipated on-die from VDD0, VDD1, VDDNB, VDDIO, VLDT, VTT and VDDA. TDP is not the maximum power of the processor. TDP values apply to operation in a triple-plane motherboard.*
4. *Power dissipated by the processor VDDIO, VTT, VLDT, and VDDA power planes only.*
5. *P-state limit when HTC is active. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors, *order# 41256 for more information.*
6. *Thermal Design Current (TDC) is the sustained current limit drawn by VDD0 and VDD1 as measured under the same conditions as TDP. Platforms should be designed to the TDC defined in the* Socket S1g2 Processor Power and Thermal Roadmap*, order# 41323 to ensure compatibility with future processors.*
7. *Specifications for multi-core processors assume equivalent P-states (voltage and frequency) and equivalent Tdie conditions for all cores. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors, *order# 41256, for details on P-state operation for multi-core processors.*
8. *Thermal Design Power dissipated by the processor VDDIO and VTT power planes only.*
9. *Assumes 50°C, minimum P-state VID_VDD and minimum P-state and a core clock divisor of 16.*
10. *Assumes VDDIO = 1.8 V and VTT = VDDIO / 2.*
11. *Assumes 35°C, minimum P-state VID_VDD, clocks stopped, HyperTransport™ links disconnected, memory in self-refresh mode, DDR2 SDRAM interface tristated.*
12. *Assumes 35°C, VDD, VDDA, and VLDT supplies are off, VDDIO and VTT are powered, memory in self-refresh mode and DDR2 SDRAM interface tristated.*
13. *Tdie Max is measured using the SB-TSI interface.*
14. *Assumes 35°C, AltVID, clocks stopped, HyperTransport™ links disconnected, memory in self-refresh mode, DDR2 SDRAM interface tristated. Not all systems are Altvid capable. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors*, order# 41256, for further details.*

3 AMD Turion™ X2 Dual-Core Mobile Processor

The following sections contain the OPN description and thermal and power specifications for the AMD Turion™ X2 dual-core mobile processor. Each column in the thermal and power tables represents a specific Ordering Part Number (OPN). Section 3.1 provides an example of the OPN structure for this processor family.

3.1 AMD Turion™ X2 Dual-Core Mobile Processor Ordering Part Number Description

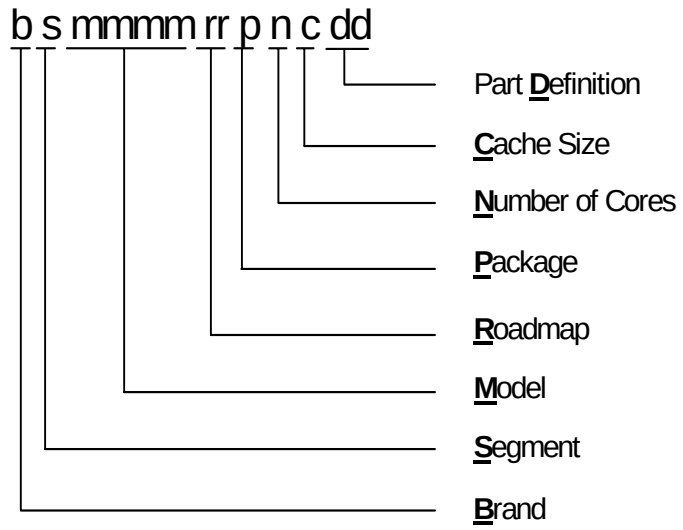

Figure 3. AMD Turion™ X2 Dual-Core Mobile Processor Ordering Part Number Diagram

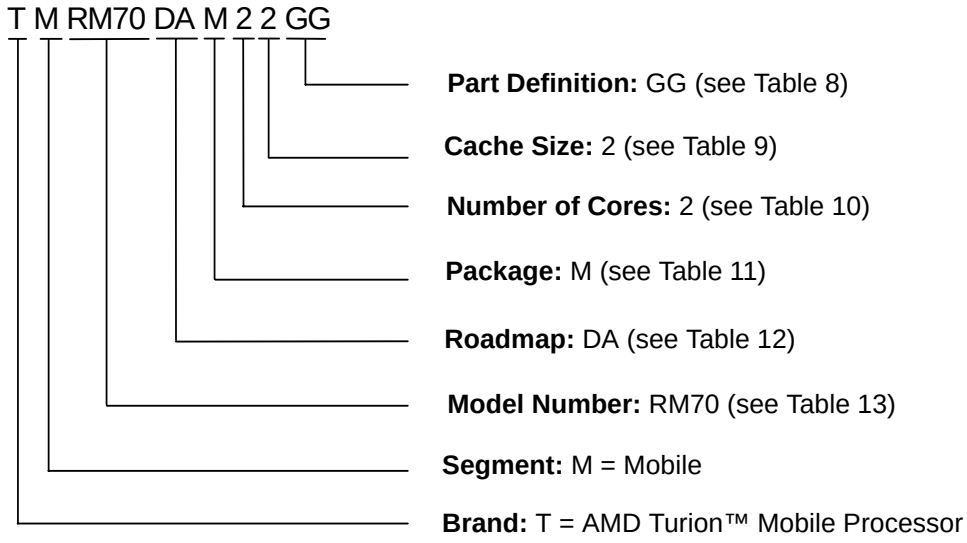

Figure 4. AMD Turion™ X2 Dual-Core Mobile Processor Ordering Part Number Example

Table 8. AMD Turion™ X2 Dual-Core Mobile Processor Part Definition Options

Part Definition	Revision	CPUID 8000_0001h EAX [31:0] (CPUID)
GG	Rev B1	00200F31h
GK	Rev B1	00200F31h

Table 9. AMD Turion™ X2 Dual-Core Mobile Processor L2 Cache Size Options

OPN Character	L2 Cache Size
2	512 KB

Table 10. AMD Turion™ X2 Dual-Core Mobile Processor Number of Cores

OPN Character	Number of Cores
2	2

Table 11. AMD Turion™ X2 Dual-Core Mobile Processor Package Options

OPN Character	Package
M	S1g2

Table 12. AMD Turion™ X2 Dual-Core Mobile Processor Roadmap Options

OPN Character	Power, Segment	Number of Cores	Socket Infrastructure
DA	35 W, Notebook	2	S1g2

Table 13. AMD Turion™ X2 Dual-Core Mobile Processor Model Number Options

Frequency	L2 Cache Size	Model Number
2000 MHz	512 KB	RM70
2100 MHz	512 KB	RM72
2200 MHz	512 KB	RM74

3.2 AMD Turion™ X2 Dual-Core Mobile Processor Thermal and Power Table Guide

The thermal and power table guide shown in Table 14 maps SOPNs and the properties associated with their defined characters to the proper thermal and power table subsections and page numbers. This table is designed to be used as a quick reference for finding the appropriate subsection for the thermal and power tables corresponding to an SOPN.

Table 14. AMD Turion™ X2 Dual-Core Mobile Processor Thermal and Power Table Guide

SOPN	Power	Revision	Thermal/Power Tables
TM mmmm **DA** pnc **GG**	35 W	Rev B1	Section 3.3.1 on page 22
TM mmmm **DA** pnc **GK**	35 W	Rev B1	Section 3.3.2 on page 24

3.3 AMD Turion™ X2 Dual-Core Mobile Processor Thermal and Power Specifications

Refer to the *AMD Family 11h Processor Electrical Data Sheet*, order# 40683, for electrical specifications for the processor. Refer to the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors*, order# 41256, for power management BIOS requirements.

Section 3.1 on page 18 provides an example of the OPN structure for processors documented in this chapter and Table 14 on page 20 provides a guide to OPN organization in the following subsections. Refer to Section 1.2 on page 9 and Section 1.3 on page 9 for numbering conventions and terminology definitions used in these tables.

3.3.1 TM mmmm DA pnc GG (35 W Mobile, S1g2) Thermal and Power Specifications

State	Specification[7]	Notes	TMRM70DAM22GG	TMRM72DAM22GG
S0.C0.Px	Tdie Max	13	100 °C	100 °C
	Tambient		0 °C to 35 °C	0 °C to 35 °C
	TRise		10 °C	10 °C
	Thermal Resistance (die-amb)		1.77 °C/W	1.57 °C/W
	Startup P-state		S0.C0.P2	S0.C0.P2
	HTC P-state Limit	5	S0.C0.HTC	S0.C0.HTC
	IDDNB Max		1.61 A	1.61 A
	VID_VDDNB		0.900 V	0.900 V
S0.C0.P0	CPU COF	1	2000 MHz	2100 MHz
	TDP	3,6	31.0 W	35.0 W
	VID_VDD Min	2	1.075 V	1.075 V
	VID_VDD Max	2	1.125 V	1.125 V
	TDC	6	24.7 A	28.4 A
S0.C0.P1	CPU COF	1	1000 MHz	1050 MHz
	TDP	3,6	15.3 W	16.0 W
	VID_VDD Min	2	0.950 V	0.950 V
	VID_VDD Max	2	0.950 V	0.950 V
	TDC	6	11.4 A	12.2 A
S0.C0.P2	CPU COF	1	500 MHz	525 MHz
	TDP	3,6	9.2 W	9.1 W
	VID_VDD Min	2	0.800 V	0.800 V
	VID_VDD Max	2	0.800 V	0.800 V
	TDC	6	5.9 A	5.9 A
S0.C0.HTC	CPU COF	1	750 MHz	800 MHz
	TDP	3,6	22.1 W	24.5 W
	VID_VDD Min	2	1.200 V	1.200 V
	VID_VDD Max	2	1.200 V	1.200 V
	TDC	6	14.7 A	16.7 A
	C1 Halt	9		
	IDD Max		1.19 A	1.19 A
	IDDNB Max		1.61 A	1.61 A
	I/O Power	4,10	3.0 W	3.0 W
	C1E/S1 @ Min P-state	11		
	IDD Max		0.84 A	0.84 A
	IDDNB Max		0.14 A	0.14 A
	I/O Power	4,10	300 mW	300 mW
	C1E/S1 Altvid	14		
	IDD Max		0.69 A	0.69 A
	IDDNB Max		0.14 A	0.14 A
	I/O Power	4,10	300 mW	300 mW
	S3	12		
	I/O Power	8	150 mW	150 mW

The notes for this table are on page 25.

State	Specification[7]	Notes	TMRM74DAM22GG
S0.C0.Px	Tdie Max	13	100 °C
	Tambient		0 °C to 35 °C
	TRise		10 °C
	Thermal Resistance (die-amb)		1.57 °C/W
	Startup P-state		S0.C0.P2
	HTC P-state Limit	5	S0.C0.HTC
	IDDNB Max		1.61 A
	VID_VDDNB		0.900 V
S0.C0.P0	CPU COF	1	2200 MHz
	TDP	3,6	35.0 W
	VID_VDD Min	2	1.075 V
	VID_VDD Max	2	1.125 V
	TDC	6	28.4 A
S0.C0.P1	CPU COF	1	1100 MHz
	TDP	3,6	16.1 W
	VID_VDD Min	2	0.950 V
	VID_VDD Max	2	0.950 V
	TDC	6	12.3 A
S0.C0.P2	CPU COF	1	550 MHz
	TDP	3,6	9.1 W
	VID_VDD Min	2	0.800 V
	VID_VDD Max	2	0.800 V
	TDC	6	5.8 A
S0.C0.HTC	CPU COF	1	850 MHz
	TDP	3,6	24.5 W
	VID_VDD Min	2	1.200 V
	VID_VDD Max	2	1.200 V
	TDC	6	16.7 A
	C1 Halt	9	
	IDD Max		1.19 A
	IDDNB Max		1.61 A
	I/O Power	4,10	3.0 W
	C1E/S1 @ Min P-state	11	
	IDD Max		0.84 A
	IDDNB Max		0.14 A
	I/O Power	4,10	300 mW
	C1E/S1 Altvid	14	
	IDD Max		0.69 A
	IDDNB Max		0.14 A
	I/O Power	4,10	300 mW
	S3	12	
	I/O Power	8	150 mW

The notes for this table are on page 25.

3.3.2 TM mmmm DA pnc GK (35 W Mobile, S1g2) Thermal and Power Specifications

State	Specification[7]	Notes	TMRM70DAM22GK
S0.C0.Px	Tdie Max	13	100 °C
	Tambient		0 °C to 35 °C
	TRise		10 °C
	Thermal Resistance (die-amb)		1.57 °C/W
	Startup P-state		S0.C0.P2
	HTC P-state Limit	5	S0.C0.HTC
	IDDNB Max		1.61 A
	VID_VDDNB		0.900 V
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3,6	35.0 W
	VID_VDD Min	2	1.075 V
	VID_VDD Max	2	1.125 V
	TDC	6	28.4 A
S0.C0.P1	CPU COF	1	1000 MHz
	TDP	3,6	15.8 W
	VID_VDD Min	2	0.950 V
	VID_VDD Max	2	0.950 V
	TDC	6	11.9 A
S0.C0.P2	CPU COF	1	500 MHz
	TDP	3,6	9.1 W
	VID_VDD Min	2	0.800 V
	VID_VDD Max	2	0.800 V
	TDC	6	5.8 A
S0.C0.HTC	CPU COF	1	750 MHz
	TDP	3,6	24.5 W
	VID_VDD Min	2	1.200 V
	VID_VDD Max	2	1.200 V
	TDC	6	16.7 A
	C1 Halt	9	
	IDD Max		1.19 A
	IDDNB Max		1.61 A
	I/O Power	4,10	3.0 W
	C1E/S1 @ Min P-state	11	
	IDD Max		0.84 A
	IDDNB Max		0.14 A
	I/O Power	4,10	300 mW
	C1E/S1 Altvid	14	
	IDD Max		0.69 A
	IDDNB Max		0.14 A
	I/O Power	4,10	300 mW
	S3	12	
	I/O Power	8	150 mW

The notes for this table are on page 25.

AMD Turion™ X2 Dual-Core Mobile Processor Thermal and Power Specification Table Notes:

1. *Frequency reported to the OS is rounded to the nearest 100-MHz boundary.*
2. *Variable voltage—any valid voltage between VDD min and VDD max is allowed.*
3. *The processor thermal solution should be designed to accommodate thermal design power (TDP) at Tdie,max. TDP is measured under the conditions of all cores operating at CPU COF, Tdie Max, and VDD at the voltage requested by the processor. TDP includes all power dissipated on-die from VDD0, VDD1, VDDNB, VDDIO, VLDT, VTT and VDDA. TDP is not the maximum power of the processor. TDP values apply to operation in a triple-plane motherboard.*
4. *Power dissipated by the processor VDDIO, VTT, VLDT, and VDDA power planes only.*
5. *P-state limit when HTC is active. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors, *order# 41256 for more information.*
6. *Thermal Design Current (TDC) is the sustained current limit drawn by VDD0 and VDD1 as measured under the same conditions as TDP. Platforms should be designed to the TDC defined in the* Socket S1g2 Processor Power and Thermal Roadmap*, order# 41323 to ensure compatibility with future processors.*
7. *Specifications for multi-core processors assume equivalent P-states (voltage and frequency) and equivalent Tdie conditions for all cores. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors, *order# 41256, for details on P-state operation for multi-core processors.*
8. *Thermal Design Power dissipated by the processor VDDIO and VTT power planes only.*
9. *Assumes 50°C, minimum P-state VID_VDD and minimum P-state and a core clock divisor of 16.*
10. *Assumes VDDIO = 1.8 V and VTT = VDDIO / 2.*
11. *Assumes 35°C, minimum P-state VID_VDD, clocks stopped, HyperTransport™ links disconnected, memory in self-refresh mode, DDR2 SDRAM interface tristated.*
12. *Assumes 35°C, VDD, VDDA, and VLDT supplies are off, VDDIO and VTT are powered, memory in self-refresh mode and DDR2 SDRAM interface tristated.*
13. *Tdie Max is measured using the SB-TSI interface.*
14. *Assumes 35°C, AltVID, clocks stopped, HyperTransport™ links disconnected, memory in self-refresh mode, DDR2 SDRAM interface tristated. Not all systems are Altvid capable. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors*, order# 41256, for further details.*

4 AMD Athlon™ X2 Dual-Core Processor

The following sections contain the OPN description and thermal and power specifications for the AMD Athlon™ X2 dual-core processor. Each column in the thermal and power tables represents a specific Ordering Part Number (OPN). Section 4.1 provides an example of the OPN structure for this processor family.

4.1 AMD Athlon™ X2 Dual-Core Processor Ordering Part Number Description

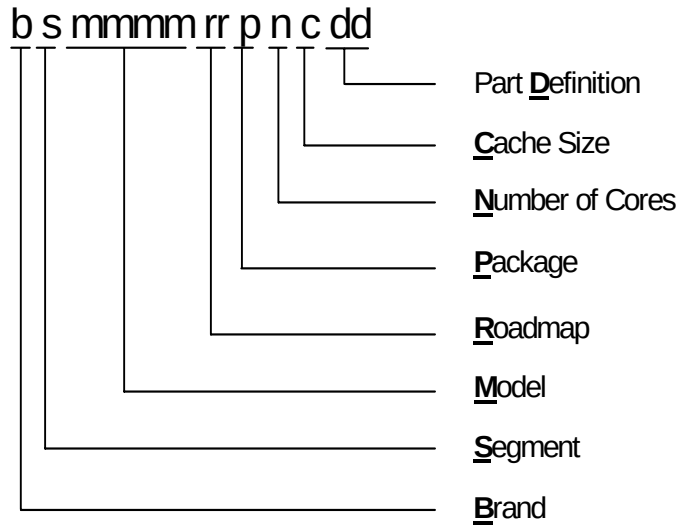

Figure 5. AMD Athlon™ X2 Dual-Core Processor Ordering Part Number Diagram

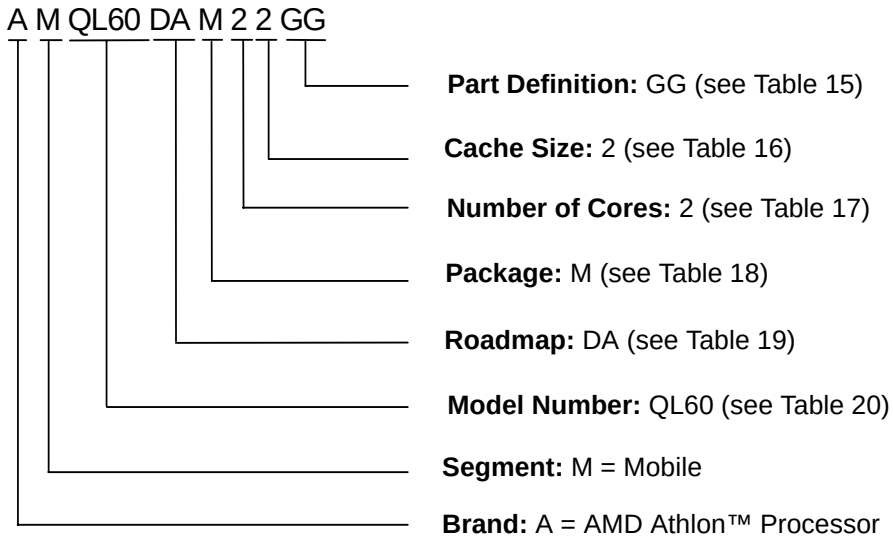

Figure 6. AMD Athlon™ X2 Dual-Core Processor Ordering Part Number Example

Table 15. AMD Athlon™ X2 Dual-Core Processor Part Definition Options

Part Definition	Revision	CPUID 8000_0001h EAX [31:0] (CPUID)
GG	Rev B1	00200F31h

Table 16. AMD Athlon™ X2 Dual-Core Processor L2 Cache Size Options

OPN Character	L2 Cache Size
2	512 KB

Table 17. AMD Athlon™ X2 Dual-Core Processor Number of Cores

OPN Character	Number of Cores
2	2

Table 18. AMD Athlon™ X2 Dual-Core Processor Package Options

OPN Character	Package
M	S1g2

Table 19. AMD Athlon™ X2 Dual-Core Processor Roadmap Options

OPN Character	Power, Segment	Number of Cores	Socket Infrastructure
DA	35 W, Notebook	2	S1g2

Table 20. AMD Athlon™ X2 Dual-Core Processor Model Number Options

Frequency	L2 Cache Size	Model Number
1900 MHz	512 KB	QL60
2000 MHz	512 KB	QL62
2100 MHz	512 KB	QL64

4.2 AMD Athlon™ X2 Dual-Core Processor Thermal and Power Table Guide

The thermal and power table guide shown in Table 21 maps SOPNs and the properties associated with their defined characters to the proper thermal and power table subsections and page numbers. This table is designed to be used as a quick reference for finding the appropriate subsection for the thermal and power tables corresponding to an SOPN.

Table 21. AMD Athlon™ X2 Dual-Core Processor Thermal and Power Table Guide

SOPN	Power	Revision	Thermal/Power Tables
AM mmmm **DA** pnc **GG**	35 W	Rev B1	Section 4.3.1 on page 30

4.3 AMD Athlon™ X2 Dual-Core Processor Thermal and Power Specifications

Refer to the *AMD Family 11h Processor Electrical Data Sheet*, order# 40683, for electrical specifications for the processor. Refer to the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors*, order# 41256, for power management BIOS requirements.

Section 4.1 on page 26 provides an example of the OPN structure for processors documented in this chapter and Table 21 on page 28 provides a guide to OPN organization in the following subsections. Refer to Section 1.2 on page 9 and Section 1.3 on page 9 for numbering conventions and terminology definitions used in these tables.

4.3.1 AM mmmm DA pnc GG (35 W Mobile, S1g2) Thermal and Power Specifications

State	Specification[7]	Notes	AMQL60DAM22GG	AMQL62DAM22GG
S0.C0.Px	Tdie Max	13	100 °C	100 °C
	Tambient		0 °C to 35 °C	0 °C to 35 °C
	TRise		10 °C	10 °C
	Thermal Resistance (die-amb)		1.57 °C/W	1.57 °C/W
	Startup P-state		S0.C0.P1	S0.C0.P1
	HTC P-state Limit	5	S0.C0.HTC	S0.C0.HTC
	IDDNB Max		1.61 A	1.61 A
	VID_VDDNB		0.900 V	0.900 V
S0.C0.P0	CPU COF	1	1900 MHz	2000 MHz
	TDP	3,6	35.0 W	35.0 W
	VID_VDD Min	2	1.075 V	1.075 V
	VID_VDD Max	2	1.125 V	1.125 V
	TDC	6	28.4 A	28.4 A
S0.C0.P1	CPU COF	1	950 MHz	1000 MHz
	TDP	3,6	18.3 W	15.8 W
	VID_VDD Min	2	0.950 V	0.950 V
	VID_VDD Max	2	0.950 V	0.950 V
	TDC	6	14.5 A	11.9 A
S0.C0.HTC	CPU COF	1	700 MHz	750 MHz
	TDP	3,6	24.8 W	24.5 W
	VID_VDD Min	2	1.200 V	1.200 V
	VID_VDD Max	2	1.200 V	1.200 V
	TDC	6	17.0 A	16.7 A
C1 Halt		9		
IDD Max			3.11 A	3.11 A
I/O Power		4,10	3.0 W	3.0 W
C1E/S1 @ Min P-state		11		
IDD Max			1.73 A	1.73 A
IDDNB Max			0.14 A	0.14 A
I/O Power		4,10	1.2 W	1.2 W
S3		12		
I/O Power		8	250 mW	250 mW

The notes for this table are on page 32.

State	Specification[7]	Notes	AMQL64DAM22GG
S0.C0.Px	Tdie Max	13	100 °C
	Tambient		0 °C to 35 °C
	TRise		10 °C
	Thermal Resistance (die-amb)		1.57 °C/W
	Startup P-state		S0.C0.P1
	HTC P-state Limit	5	S0.C0.HTC
	IDDNB Max		1.61 A
	VID_VDDNB		0.900 V
S0.C0.P0	CPU COF	1	2100 MHz
	TDP	3,6	35.0 W
	VID_VDD Min	2	1.075 V
	VID_VDD Max	2	1.125 V
	TDC	6	28.4 A
S0.C0.P1	CPU COF	1	1050 MHz
	TDP	3,6	16.0 W
	VID_VDD Min	2	0.950 V
	VID_VDD Max	2	0.950 V
	TDC	6	12.1 A
S0.C0.HTC	CPU COF	1	800 MHz
	TDP	3,6	24.5 W
	VID_VDD Min	2	1.200 V
	VID_VDD Max	2	1.200 V
	TDC	6	16.7 A
	C1 Halt	9	
	IDD Max		3.11 A
	I/O Power	4,10	3.0 W
	C1E/S1 @ Min P-state	11	
	IDD Max		1.73 A
	IDDNB Max		0.14 A
	I/O Power	4,10	1.2 W
	S3	12	
	I/O Power	8	250 mW

The notes for this table are on page 32.

AMD Athlon™ X2 Dual-Core Processor Thermal and Power Specification Table Notes:

1. *Frequency reported to the OS is rounded to the nearest 100-MHz boundary.*
2. *Variable voltage—any valid voltage between VDD min and VDD max is allowed.*
3. *The processor thermal solution should be designed to accommodate thermal design power (TDP) at Tdie,max. TDP is measured under the conditions of all cores operating at CPU COF, Tdie Max, and VDD at the voltage requested by the processor. TDP includes all power dissipated on-die from VDD0, VDD1, VDDNB, VDDIO, VLDT, VTT and VDDA. TDP is not the maximum power of the processor. TDP values apply to operation in a triple-plane motherboard.*
4. *Power dissipated by the processor VDDIO, VTT, VLDT, and VDDA power planes only.*
5. *P-state limit when HTC is active. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors, *order# 41256, for more information.*
6. *Thermal Design Current (TDC) is the sustained current limit drawn by VDD0 and VDD1 as measured under the same conditions as TDP. Platforms should be designed to the TDC defined in the* Socket S1g2 Processor Power and Thermal Roadmap*, order# 41323 to ensure compatibility with future processors.*
7. *Specifications for multi-core processors assume equivalent P-states (voltage and frequency) and equivalent Tdie conditions for all cores. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors, *order# 41256, for details on P-state operation for multi-core processors.*
8. *Thermal Design Power dissipated by the processor VDDIO and VTT power planes only.*
9. *Assumes 50°C, minimum P-state VID_VDD and minimum P-state and a core clock divisor of 16.*
10. *Assumes VDDIO = 1.8 V and VTT = VDDIO / 2.*
11. *Assumes 35°C, minimum P-state VID_VDD, clock divider set to 512, HyperTransport™ links disconnected, memory in self-refresh mode, DDR2 SDRAM interface tristated.*
12. *Assumes 35°C, VDD, VDDA, and VLDT supplies are off, VDDIO and VTT are powered, memory in self-refresh mode and DDR2 SDRAM interface tristated.*
13. *Tdie Max is measured using the SB-TSI interface.*

5 AMD Sempron™ Processor

The following sections contain the OPN description and thermal and power specifications for the AMD Sempron™ processor. Each column in the thermal and power tables represents a specific Ordering Part Number (OPN). Section 5.1 provides an example of the OPN structure for this processor family.

5.1 AMD Sempron™ Processor Ordering Part Number Description

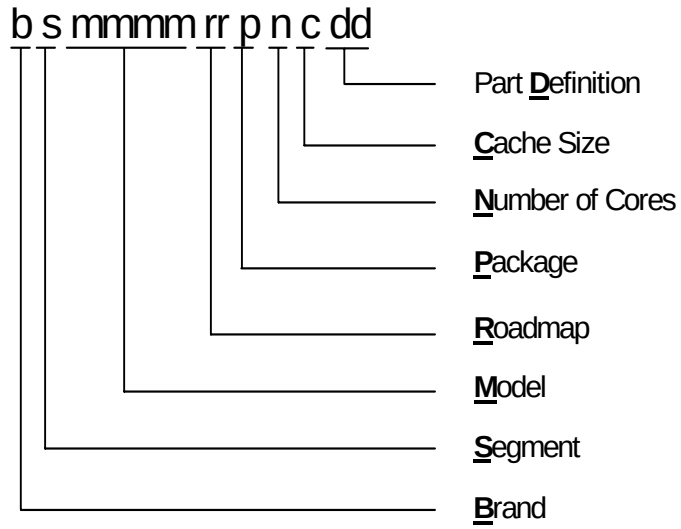

Figure 7. AMD Sempron™ Processor Ordering Part Number Diagram

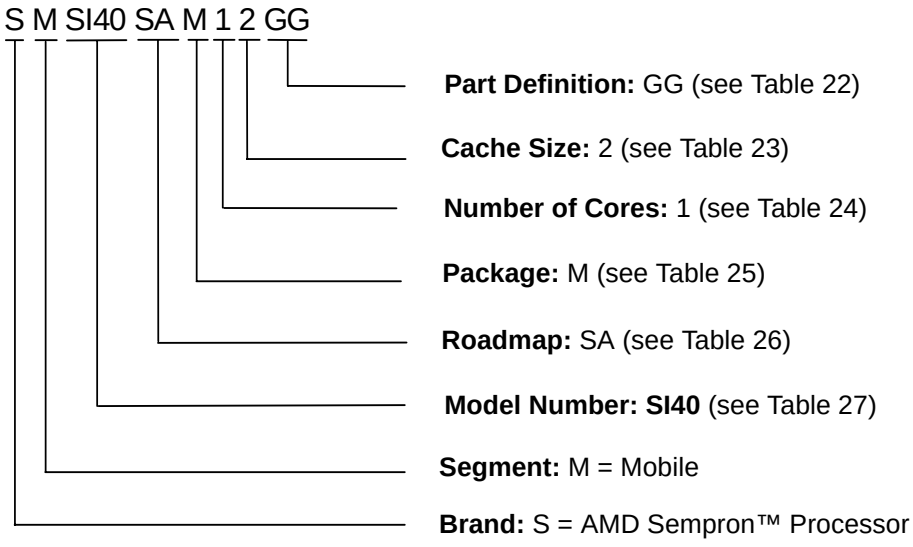

Figure 8. AMD Sempron™ Processor Ordering Part Number Example

Table 22. AMD Sempron™ Processor Part Definition Options

Part Definition	Revision	CPUID 8000_0001h EAX [31:0] (CPUID)
GG	Rev B1	00200F31h

Table 23. AMD Sempron™ Processor L2 Cache Size Options

OPN Character	L2 Cache Size
1	256 KB
2	512 KB

Table 24. AMD Sempron™ Processor Number of Cores

OPN Character	Number of Cores
1	1
2	2

Table 25. AMD Sempron™ Processor Package Options

OPN Character	Package
M	S1g2

Table 26. AMD Sempron™ Processor Roadmap Options

OPN Character	Power, Segment	Number of Cores	Socket Infrastructure
SA	25 W, Notebook	1	S1g2
DA	35 W, Notebook	2	S1g2

Table 27. AMD Sempron™ Processor Model Number Options

Frequency	L2 Cache Size	Model Number
1800 MHz	512 KB	NI52
2000 MHz	512 KB	SI40

5.2 AMD Sempron™ Processor Thermal and Power Table Guide

The thermal and power table guide shown in Table 28 maps SOPNs and the properties associated with their defined characters to the proper thermal and power table subsections and page numbers. This table is designed to be used as a quick reference for finding the appropriate subsection for the thermal and power tables corresponding to an SOPN.

Table 28. AMD Sempron™ Processor Thermal and Power Table Guide

SOPN	Power	Revision	Thermal/Power Tables
SM mmmm **SA** pnc **GG**	25 W	Rev B1	Section 5.3.1 on page 37
SM mmmm **DA** pnc **GG**	35 W	Rev B1	Section 5.3.2 on page 38

5.3 AMD Sempron™ Processor Thermal and Power Specifications

Refer to the *AMD Family 11h Processor Electrical Data Sheet*, order# 40683, for electrical specifications for the processor. Refer to the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors*, order# 41256, for power management BIOS requirements.

Section 5.1 on page 33 provides an example of the OPN structure for processors documented in this chapter and Table 28 on page 35 provides a guide to OPN organization in the following subsections. Refer to Section 1.2 on page 9 and Section 1.3 on page 9 for numbering conventions and terminology definitions used in these tables.

5.3.1 SM mmmm SA pnc GG (25 W Mobile, S1g2) Thermal and Power Specifications

State	Specification	Notes	SMSI40SAM12GG	SMSI42SAM12GG
S0.C0.Px	Tdie Max	13	100 °C	100 °C
	Tambient		0 °C to 35 °C	0 °C to 35 °C
	TRise		10 °C	10 °C
	Thermal Resistance (die-amb)		2.20 °C/W	2.20 °C/W
	Startup P-state		S0.C0.P1	S0.C0.P1
	HTC P-state Limit	5	S0.C0.HTC	S0.C0.HTC
	IDDNB Max		1.61 A	1.61 A
	VID_VDDNB		0.900 V	0.900 V
S0.C0.P0	CPU COF	1	2000 MHz	2100 MHz
	TDP	3,6,14	25.0 W	25.0 W
	VID_VDD Min	2	1.075 V	1.075 V
	VID_VDD Max	2	1.125 V	1.125 V
	TDC	6	19.1 A	19.1 A
S0.C0.P1	CPU COF	1	1000 MHz	1050 MHz
	TDP	3,6,14	14.1 W	12.8 W
	VID_VDD Min	2	0.950 V	0.950 V
	VID_VDD Max	2	0.950 V	0.950 V
	TDC	6	10.2 A	8.8 A
S0.C0.HTC	CPU COF	1	750 MHz	800 MHz
	TDP	3,6,14	17.8 W	17.6 W
	VID_VDD Min	2	1.200 V	1.200 V
	VID_VDD Max	2	1.200 V	1.200 V
	TDC	6	11.1 A	11.0 A
	C1 Halt	9		
	IDD Max		1.53 A	1.53 A
	I/O Power	4,10	3.0 W	3.0 W
	C1E/S1 @ Min P-state	11		
	IDD Max		1.09 A	1.09 A
	I/O Power	4,10	1.2 W	1.2 W
	S3	12		
	I/O Power	8	250 mW	250 mW

The notes for this table are on page 39.

5.3.2 SM mmmm DA pnc GG (35 W Mobile, S1g2) Thermal and Power Specifications

State	Specification[7]	Notes	SMNI52DAM21GG
S0.C0.Px	Tdie Max	13	100 °C
	Tambient		0 °C to 35 °C
	TRise		10 °C
	Thermal Resistance (die-amb)		1.57 °C/W
	Startup P-state		S0.C0.P1
	HTC P-state Limit	5	S0.C0.HTC
	IDDNB Max		1.61 A
	VID_VDDNB		0.900 V
S0.C0.P0	CPU COF	1	1800 MHz
	TDP	3,6	35.0 W
	VID_VDD Min	2	1.075 V
	VID_VDD Max	2	1.150 V
	TDC	6	28.4 A
S0.C0.P1	CPU COF	1	900 MHz
	TDP	3,6	15.5 W
	VID_VDD Min	2	0.950 V
	VID_VDD Max	2	0.950 V
	TDC	6	11.6 A
S0.C0.HTC	CPU COF	1	650 MHz
	TDP	3,6	24.5 W
	VID_VDD Min	2	1.200 V
	VID_VDD Max	2	1.200 V
	TDC	6	16.7 A
	C1 Halt	9	
	IDD Max		3.32 A
	I/O Power	4,10	3.0 W
	C1E/S1 @ Min P-state	11	
	IDD Max		1.83 A
	I/O Power	4,10	1.2 W
	S3	12	
	I/O Power	8	250 mW

The notes for this table are on page 39.

AMD Sempron™ Processor Thermal and Power Specification Table Notes:

1. *Frequency reported to the OS is rounded to the nearest 100-MHz boundary.*
2. *Variable voltage—any valid voltage between VDD min and VDD max is allowed.*
3. *The processor thermal solution should be designed to accommodate thermal design power (TDP) at Tdie,max. TDP is measured under the conditions of all cores operating at CPU COF, Tdie Max, and VDD at the voltage requested by the processor. TDP includes all power dissipated on-die from VDD0, VDD1, VDDNB, VDDIO, VLDT, VTT and VDDA. TDP is not the maximum power of the processor. TDP values apply to operation in a triple-plane motherboard.*
4. *Power dissipated by the processor VDDIO, VTT, VLDT, and VDDA power planes only.*
5. *P-state limit when HTC is active. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors, *order# 41256, for more information.*
6. Thermal Design Current (TDC) is the sustained current limit drawn by VDD0 and VDD1 as measured under the same conditions as TDP. Platforms should be designed to the TDC defined in the Socket S1g2 Processor Power and Thermal Roadmap, order# 41323 to ensure compatibility with future processors.
7. Specifications for multi-core processors assume equivalent P-states (voltage and frequency) and equivalent Tdie conditions for all cores. Refer to the BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors, order# 41256, for details on P-state operation for multi-core processors.
8. Thermal Design Power dissipated by the processor VDDIO and VTT power planes only.
9. Assumes 50°C, minimum P-state VID_VDD and minimum P-state and a core clock divisor of 16.
10. Assumes VDDIO = 1.8 V and VTT = VDDIO / 2.
11. Assumes 35°C, minimum P-state VID_VDD, clock divider set to 512, HyperTransport™ links disconnected, memory in self-refresh mode, DDR2 SDRAM interface tristated.
12. Assumes 35°C, VDD, VDDA, and VLDT supplies are off, VDDIO and VTT are powered, memory in self-refresh mode and DDR2 SDRAM interface tristated.
13. Tdie Max is measured using the SB-TSI interface.
14. TDP values apply to operation in a triple-plane motherboard In which each voltage plane is running at the voltage requested by the processor.

6 Power Supply Specifications

6.1 bsmmmmrr M ncdd - Socket S1 Power Supply Operating Conditions

Table 29. bsmmmmrr M ncdd VDD0 and VDD1 Power Supply DC Operating Conditions

Symbol	Parameter	Units	Min	Typ	Max	Notes
VID_VDD	VID-Requested VDD0, VDD1 Supply Level	V	Refer to the thermal/power tables under the appropriate SOPN section for this OPN specific parameter.			1
VDD_dc	DC Tolerance - VDD0, VDD1 Supply Voltage	V	VID_VDD –25 mV	VID_VDD	VID_VDD + 25 mV	
VDD_PON	Metal Mask VID	V	1.05	1.10	1.25	2
VDDNB_dc	VDDNB Supply voltage	V	VID_VDDNB –25 mV	VID_VDDNB	VID_VDDNB + 25 mV	
VID_VDDNB	VDDNB Supply voltage	V	Refer to the thermal/power tables under the appropriate SOPN section for this OPN specific parameter.			1
VDDNB_PON	Metal Mask VDDNB	V	1.05	1.10	1.25	2

Notes:

1) The processor drives a VID code corresponding to this voltage.

2) After PWROK assertion, the VID signals change from the Metal Mask VID to the value programmed during device manufacturing.

Table 30. bsmmmmrr M ncdd VDD0 and VDD1 Power Supply AC Operating Conditions

VDD_ac	VDD0, VDD1 Supply Voltage	V	VID_VDD –125 mV	VID_VDD	VID_VDD + 125 mV	1
VDDNB_ac	VDDNB Supply Voltage	V	VID_VDDNB –100 mV	VID_VDDNB	VID_VDDNB + 100 mV	2

Notes:

1) The voltage set-point must be contained within the DC specification in order to help ensure proper operation. Voltage ripple and transient events outside the DC specification must remain within the AC specification at all times. Transients above VDD_dc max must return to within the DC specification within 20 µS. Test by differentially probing the VDD0_FB_H/L and VDD1_FB_H/L signals using 20-MHz scope bandwidth limit.

2) The voltage set-point must be contained within the DC specification in order to help ensure proper operation. Voltage ripple and transient events outside the DC specification must remain within the AC specification at all times. Transients above VDDNB_dc max must return to within the DC specification within 20 µS. Test by differentially probing the VDDNB_FB_H/L signals using 20-MHz scope bandwidth limit.

Table 31. bsmmmmrr M ncdd AC and DC Operating Conditions for non-VDD Power Supplies

Symbol	Parameter	Units	Min	Typ	Max	Notes
VDDIO_dc	VDDIO Supply Voltage for DDR2 electricals	V	1.70	1.80	1.90	7
VDDIO_ac	VDDIO Supply voltage	V	VDDIO_dc –150 mV	VDDIO_dc	VDDIO_dc +150 mV	5, 6
VLDT	VLDT Supply Voltage	V	1.14	1.20	1.26	
VTT_dc	VTT Supply Voltage for DDR2 electricals	V	0.85	0.90	0.95	8
VTT_ac	VTT Supply Voltage	V	VTT_dc –75 mV	VTT_dc	VTT_dc +75 mV	5, 6
VDDA	VDDA Supply Voltage	V	2.40	2.50	2.60	
IDDIO1	VDDIO Power Supply Current	A			2.00	3, 9
ITT1	VTT Power Supply Current	mA			750	2, 4, 9
ILDT	VLDT Power Supply Current	A			1.5	1, 9
IDDA	VDDA Power Supply Current	mA			40	9

Notes:

1) ILDT is specified for one 16x16-bit Gen3 link.

2) VTT must both sink and source current.

3) VDDIO current is consumed by I, O, I/O switching current and on-chip functions (PDL, DLL, level-shifters, etc.).

4) VTT current is consumed by I, O, I/O switching current and on-chip functions (PDL, DLL, level-shifters, etc.).

5) VDDIO_ac and VTT_ac parameters are measured over a 60 second time frame with all data bus bits switching.

6) Power supply A/C measurements use a 20-MHz scope bandwidth limit.

7) All voltages are referenced to VSS. In order to help ensure proper functionality, DC voltage regulator must be set accordingly to ensure that VDDIO_dc level measured at the VDDIO_FB_H/L pins does not exceed the specified maximum and minimum range. As such, factors such as voltage regulator inaccuracy and IR drop must be carefully considered and compensated for. For example, if the inaccuracy and IR drop amounts to 50 mV, then the voltage regulator setting for VDDIO should not be lower than 1.75 V to avoid violating the VDDIO_dc minimum spec of 1.70 V.

*8) All voltages are referenced to VSS. Voltage regulator for VTT must be set accordingly so that VTT_dc level measured at the processor VTT_SENSE pin tracks 0.5*VDDIO_dc, and stays within the specified maximum and minimum range. Factors such as voltage regulator inaccuracy and IR drop have to be carefully considered and compensated for. For example, if the inaccuracy and IR drop amounts to 20 mV, the voltage regulator setting must be set 20 mV higher so that VTT still tracks 0.5*VDDIO_dc and stays within the range of 0.85 V and 0.95 V.*

9) This specification reflects the values published in the appropriate power roadmap document.

7 Power Limit Encoding

IddValue and IddDiv are available for each P-state in Pstate registers MSRC001_00[6B:64]. For more details, refer to the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 11h Processors*, order# 41256.

8 MTOPS

Table 32 shows the composite theoretical performance (CTP) calculations. The calculations are stated in millions of theoretical operations per second (MTOPS) and are based upon a formula in the United States Department of Commerce Export Administration Regulations 15 CFR 774 (Advisory Note 4 for Category 4).

All calculations contained herein are subject to change without notice. AMD makes no representation or warranty as to the accuracy or reliability of such calculations.

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Furthermore, AMD shall have no liability for any losses or damages including direct, indirect, special, punitive, incidental, or consequential, such as but not limited to, loss of anticipated profits or other economic loss occurring in connection with use of the calculations, even if AMD has been advised in advance of the possibility of such damages. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

Table 32. Composite Theoretical Performance (CTP) Calculations

Frequency	MTOPS Single-Core	MTOPS Dual-Core
800	2,467	4,667
900	2,775	5,250
1000	3,084	5,834
1100	3,392	6,417
1200	3,700	7,000
1300	4,009	7,584
1400	4,317	8,167
1500	4,625	8,750
1600	4,934	9,334
1700	5,242	9,917
1800	5,550	10,500
1900	5,859	11,084
2000	6,167	11,667
2100	6,475	12,250
2200	6,784	12,834
2300	7,092	13,417
2400	7,400	14,000
2500	7,709	14,584
2600	8,017	15,167
2700	8,325	15,750
2800	8,634	16,334
2900	8,942	16,917
3000	9,250	17,500

9 APP

Table 33 shows the Adjusted Peak Performance (APP) calculations ("Calculations") for the AMD Turion™ X2 Ultra dual-core mobile processor, AMD Turion™ X2 dual-core mobile processor, AMD Athlon™ X2 dual-core processor and Mobile AMD Sempron™ processor. The Calculations are stated in Millions of Weighted Teraflops (WT) and are based upon a formula in the United States Department of Commerce Export Administration Regulations 15 CFR 774 (Advisory Note 4 for Category 4).

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Table 33. Adjusted Peak Performance (APP) Calculations

Frequency	APP Single-Core	APP Dual-Core
800	0.0005	0.0010
900	0.0005	0.0011
1000	0.0006	0.0012
1100	0.0007	0.0013
1200	0.0007	0.0014
1300	0.0008	0.0016
1400	0.0008	0.0017
1500	0.0009	0.0018
1600	0.0010	0.0019
1700	0.0010	0.0020
1800	0.0011	0.0022
1900	0.0011	0.0023
2000	0.0012	0.0024
2100	0.0013	0.0025
2200	0.0013	0.0026
2300	0.0014	0.0028
2400	0.0014	0.0029
2500	0.0015	0.0030
2600	0.0016	0.0031
2700	0.0016	0.0032
2800	0.0017	0.0034
2900	0.0017	0.0035
3000	0.0018	0.0036